




Product Specification

AU OPTRONICS CORPORATION

(V) Preliminary Specifications
() Final Specifications

Module	14.0”(13.98”) HD⁺ 16:9 Color TFT-LCD with LED Backlight design
Model Name	B140RTN03.0 (H/W:3A)
Note ()	<i>LED Backlight with driving circuit design</i>

Customer	Date
	<u> </u> /2012
Checked & Approved by	Date
Note: This Specification is subject to change without notice.	

Approved by	Date
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Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2012/10/22	All	First Edition for Customer		

1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.



2. General Description

B140RTN03.0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 HD⁺, 1600(H) x 900(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are eDP(Embedded DisplayPort) interface compatible.

B140RTN03.0 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	355.22			
Active Area	[mm]	309.6 x 174.15			
Pixels H x V		1600 x 3 (RGB) x 900			
Pixel Pitch	[mm]	0.1935 x 0.1935			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally White			
White Luminance	[cd/m ²]	250 typ. (5 points average) 212 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		400 typ			
Response Time	[ms]	8 typ / 16 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	4.2 max (Include Logic and BL power)			
Weight	[Grams]	270 max.			
Physical Size Include bracket	[mm]		Min.	Typ.	Max.
		Length	319.9	320.4	320.9
		Width	204.6	205.1	205.6
		Thickness	-	-	3.0
Electrical Interface		1 Lane eDP			
Glass Thickness	[mm]	0.4			
Surface Treatment		Anti-Glare, Hardness 3H,			
Support Color		262K colors (RGB 6-bit)			



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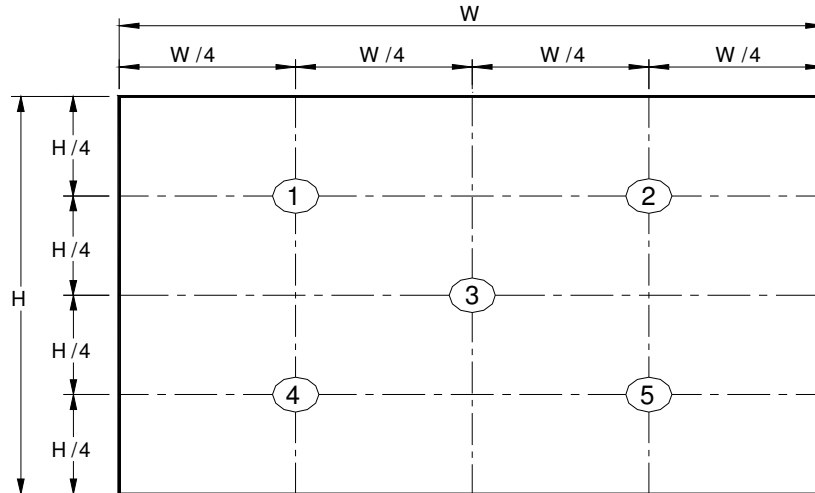
Temperature Range Operating	[°C]	0 to +50
Storage (Non-Operating)	[°C]	-20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

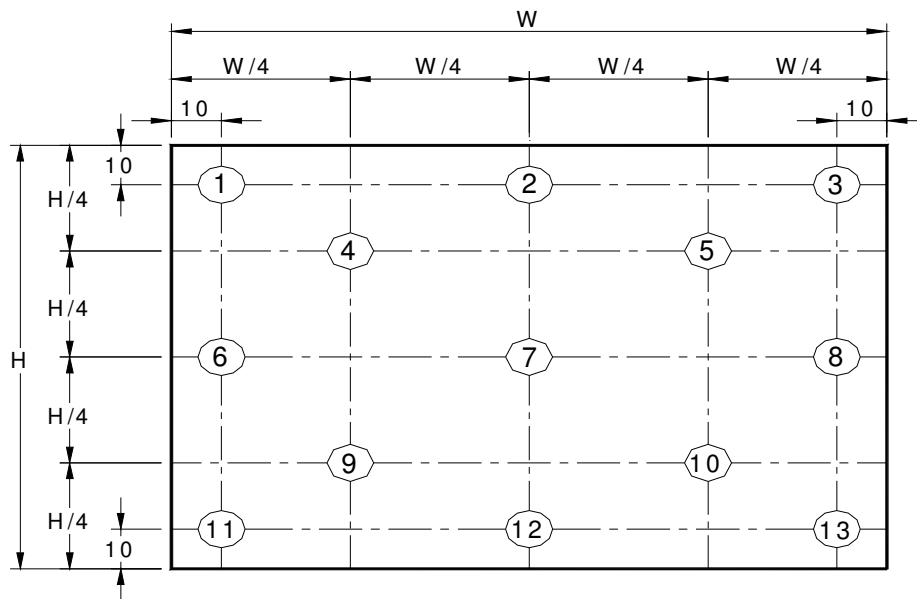
The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note			
White Luminance		5 points average	212	250	-	cd/m²	1, 4, 5.			
Viewing Angle	θ_R	Horizontal (Right) CR = 10 (Left)	40	45	-	degree	4, 9			
	θ_L		40	45	-					
	ψ_H	Vertical (Upper) CR = 10 (Lower)	10	15	-					
	ψ_L		30	35	-					
Luminance Uniformity	δ_{5P}	5 Points	-	-	1.25		1, 3, 4			
Luminance Uniformity	δ_{13P}	13 Points	-	-	1.60			2, 3, 4		
Contrast Ratio	CR		300	400	-			4, 6		
Cross talk	%		-	-	4			4, 7		
Response Time	T_{RT}	Rising + Falling	-	8	16	msec		4, 8		
Color / Chromaticity Coodinates	Red	Rx	CIE 1931			TBD	-	4		
		Ry				TBD				
	Green	Gx				TBD				
		Gy				TBD				
	Blue	Bx				TBD				
		By				TBD				
	White	Wx				0.283			0.313	0.343
		Wy				0.299			0.329	0.359
NTSC	%		-	45	-					

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

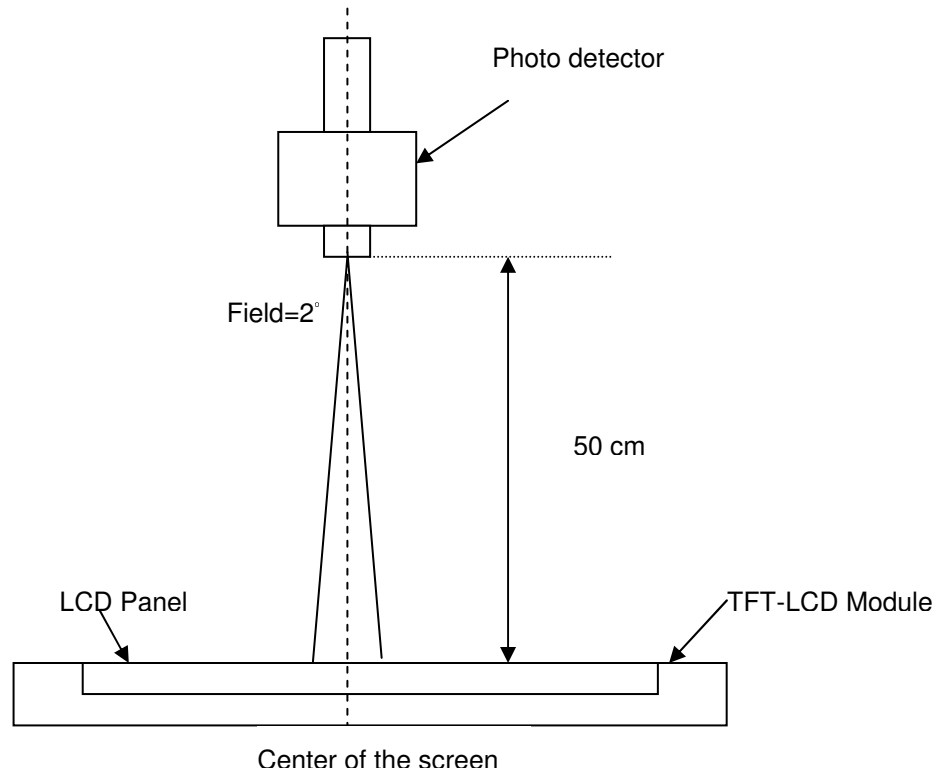
$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting

Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5 : Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points · $Y_L = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$

$L(x)$ is corresponding to the luminance of the point X at Figure in Note (1).

Note 6 : Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

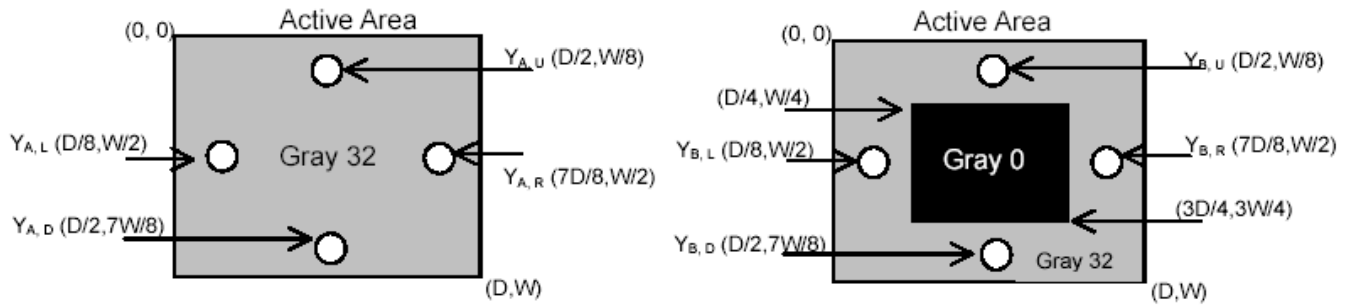
Note 7 : Definition of Cross Talk (CT)

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where

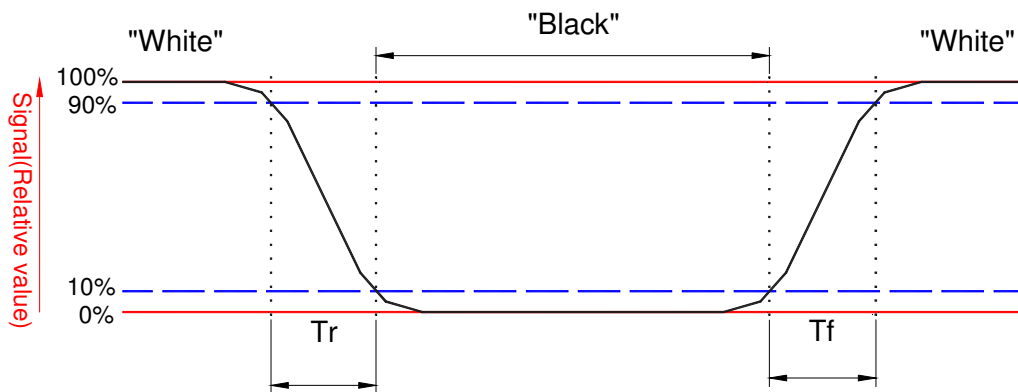
Y_A = Luminance of measured location without gray level 0 pattern (cd/m²)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m²)



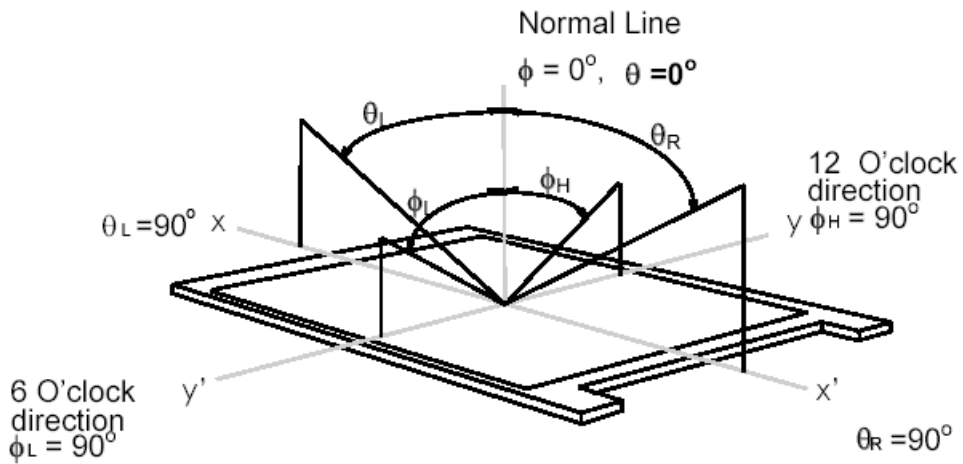
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



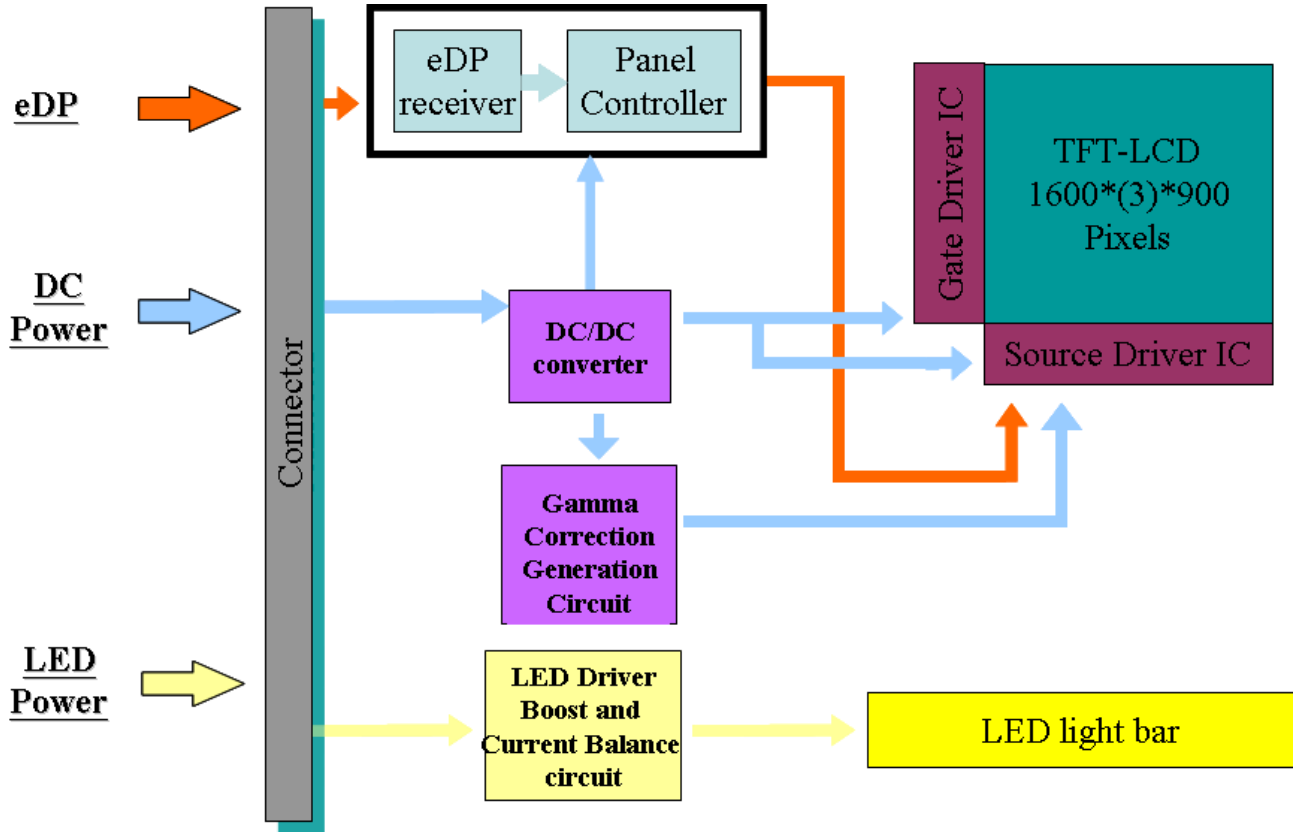
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≥ 10 , at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 14.0 inches wide Color TFT/LCD 30 Pin



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

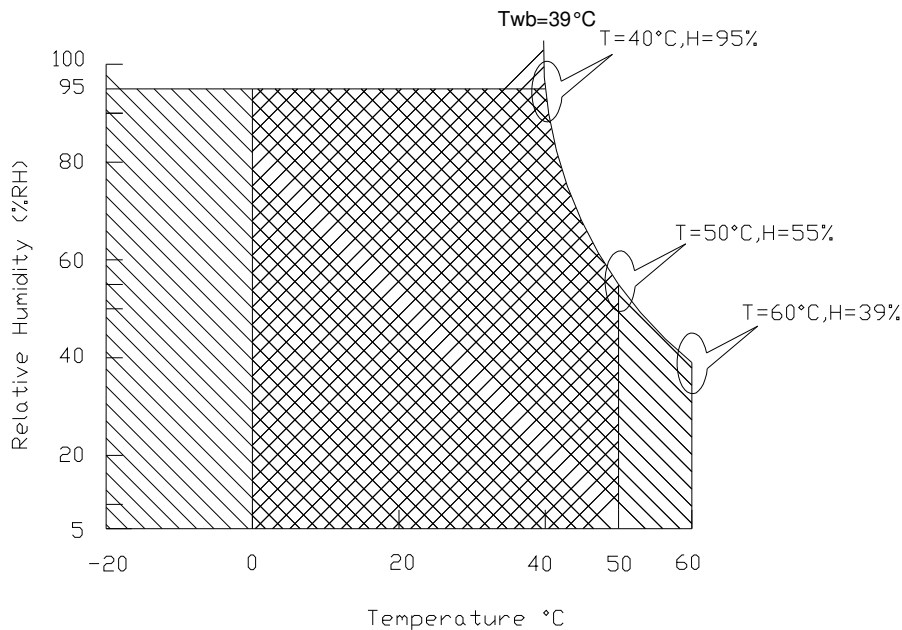
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25°C)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range

Storage Range +

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

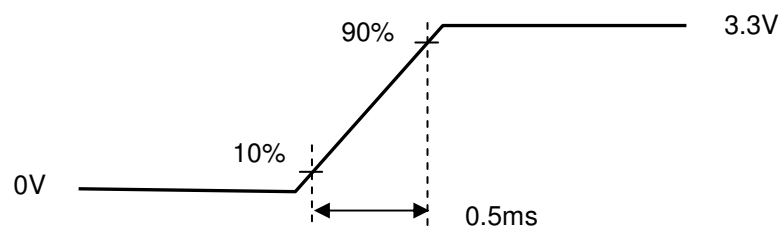
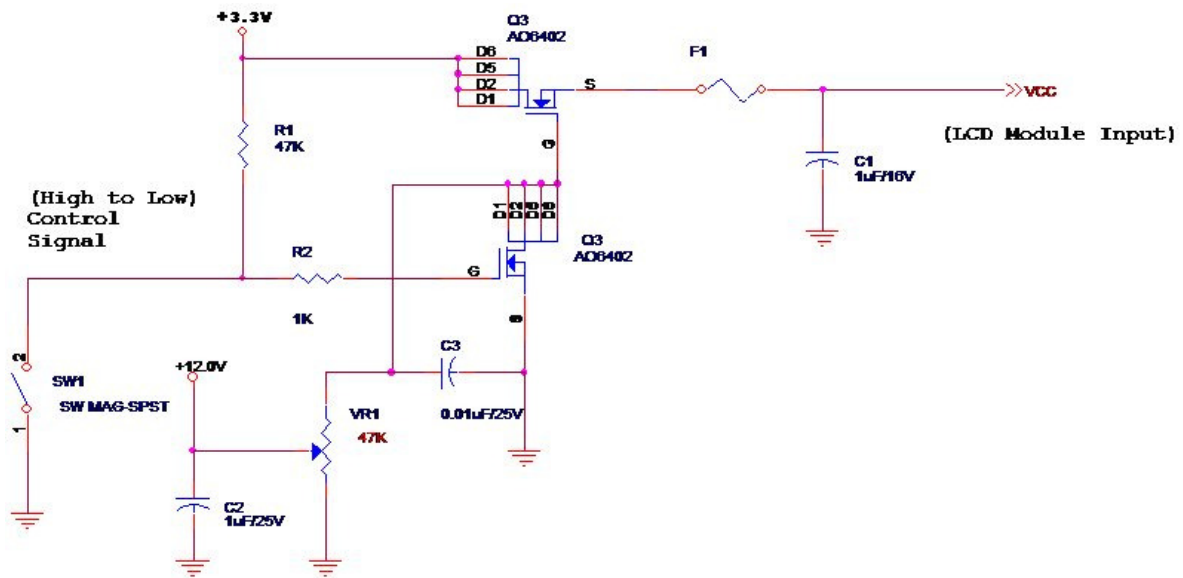
The power specification are measured under 25°C and frame frequency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power		1.1	1.25	[Watt]	Note 1
IDD	IDD Current		300	417	[mA]	Note 1
IRush	Inrush Current		-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{black}$)

Typical Measurement Condition : Mosaic Pattern

Note 2 : Measure Condition

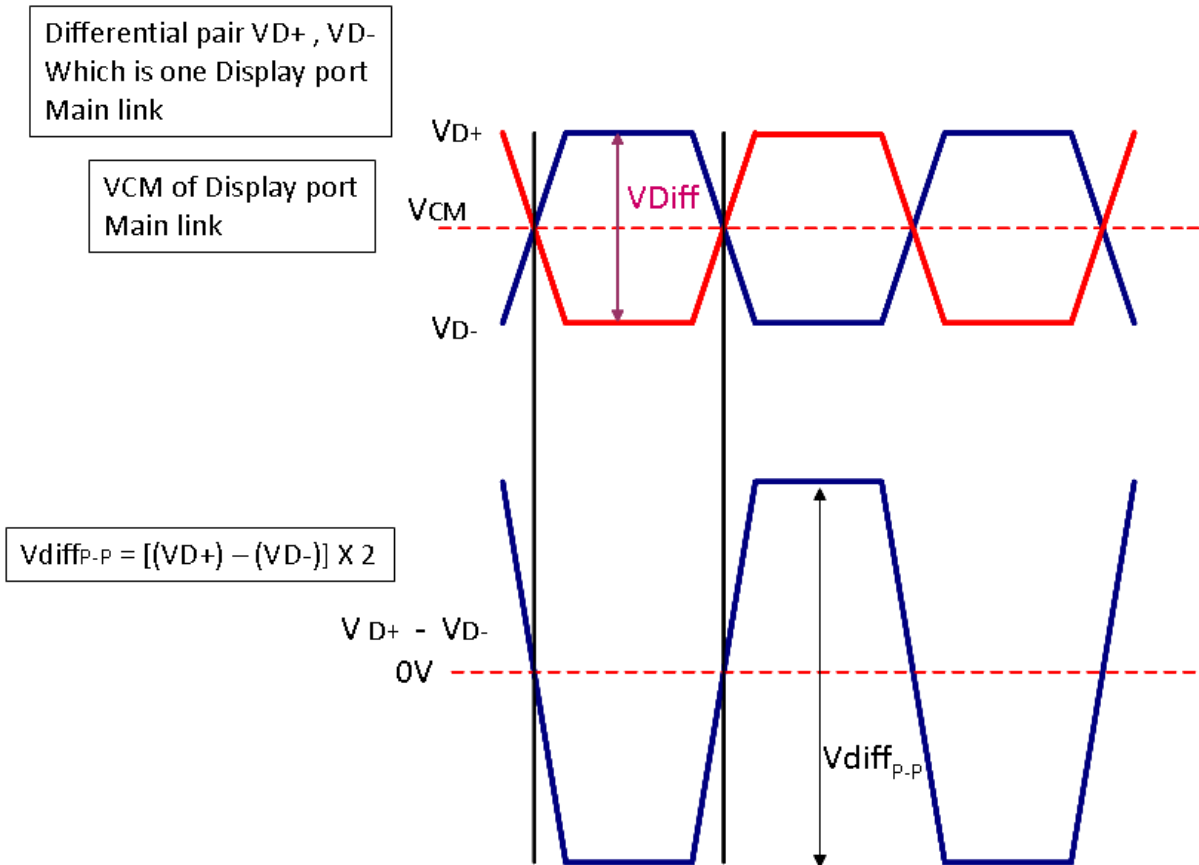


5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

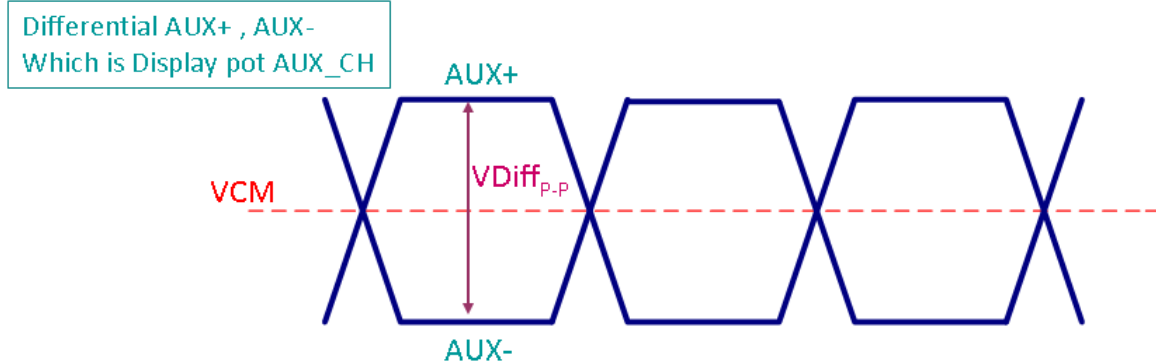
Display Port main link signal:



Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage	0.668	0.68	0.685	V
VDiff _{P-P}	Peak-to-peak Voltage at a receiving Device				mV

Fallow as VESA display port standard V1.1a

Display Port AUX_CH signal:



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	Differential Common Mode Voltage	0	VDD/2	2	V
VDiff _{p-p}	Differential peak-to-peak Voltage	0.39		1.38	V

Fallow as VESA display port standard V1.1a.

Display Port VHPD signal:

Display port VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25	-	3.6	V

Fallow as VESA display port standard V1.1a.

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED			2.9	[Watt]	(Ta=25°C), Note 1 Vin =12V
LED Life-Time	N/A	15000			Hour	(Ta=25°C), Note 2 If=21 mA

Note 1: Calculator value for reference $P_{LED} = VF$ (Normal Distribution) * I_F (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

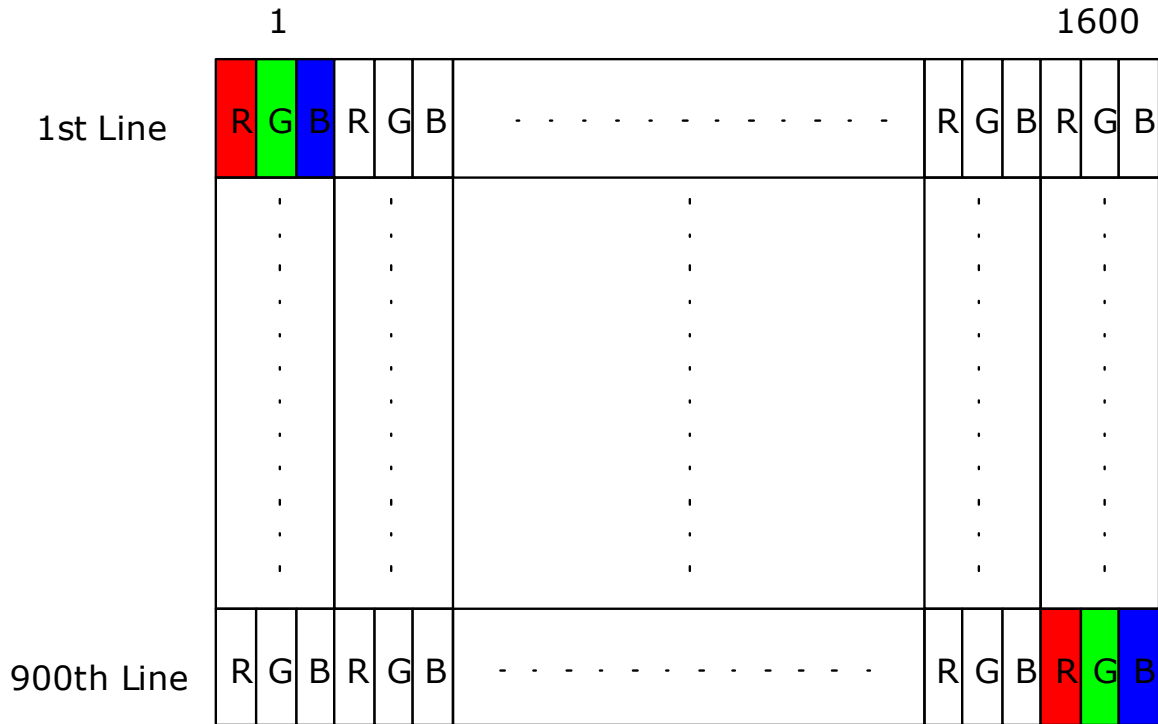
Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED				[Volt]	Define as Connector Interface (Ta=25°C)
LED Enable Input High Level	VLED_EN				[Volt]	
LED Enable Input Low Level					[Volt]	
PWM Logic Input High Level	VPWM_EN				[Volt]	
PWM Logic Input Low Level					[Volt]	
PWM Input Frequency	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty				%	

Note 1 : Recommend system pull up/down resistor no bigger than 10kohm

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.





6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

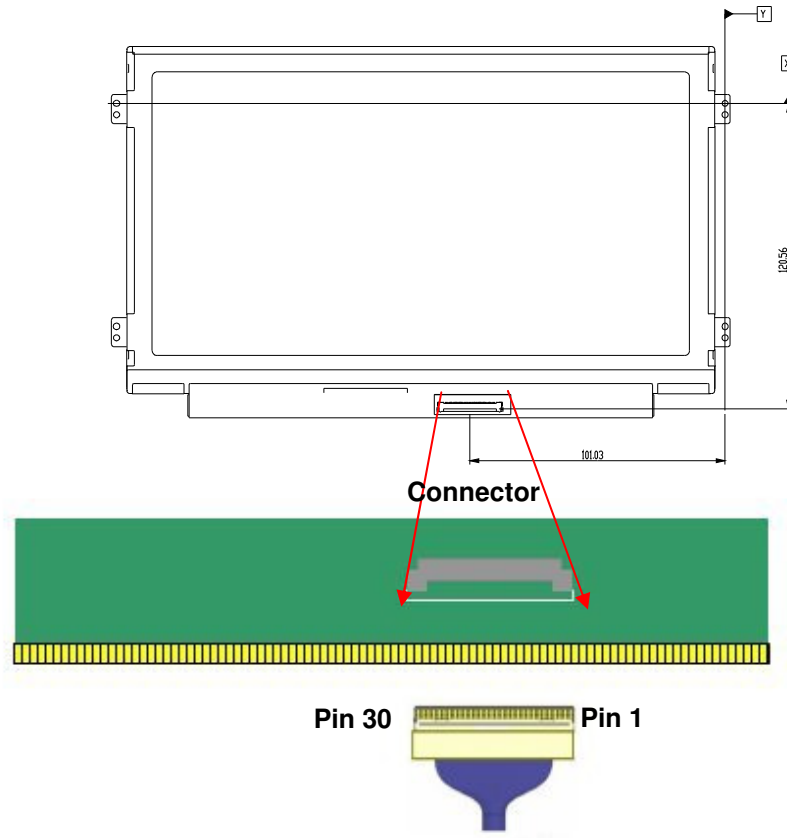
These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or compatible
Type / Part Number	I-PEX 20455-030E-12
Mating Housing/Part Number	I-PEX 20453-030T-11 or compatible

6.2.2 Pin Assignment (1 Lane)

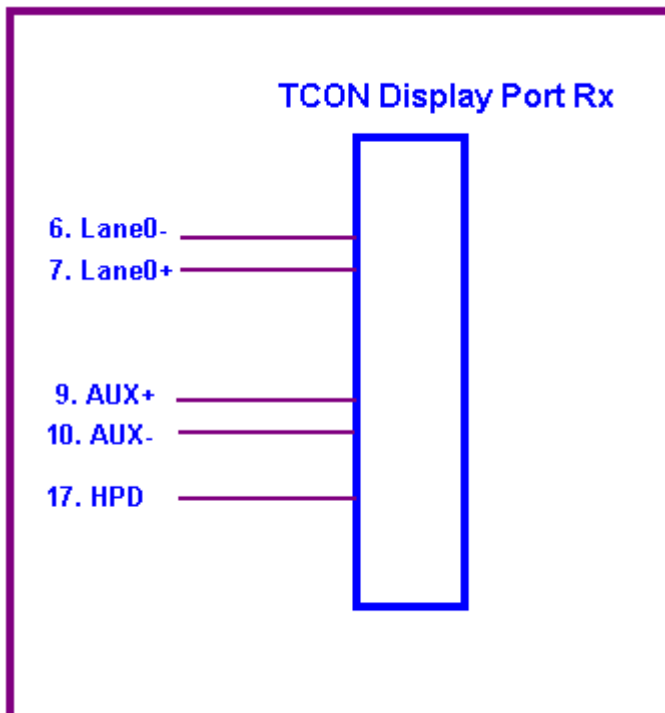
eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

PIN NO	Symbol	Function
1	NC	No Connect
2	H_GND	High Speed Ground
3	NC	
4	NC	
5	H_GND	High Speed Ground
6	Lane0_N	Comp Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Ch.
10	AUX_CH_N	Comp Signal Auxiliary Ch.
11	H_GND	High Speed Ground
12	LCD_VCC	LCD logic and driver power
13	LCD_VCC	LCD logic and driver power
14	NC	Reverse for AUO TEST only
15	LCD_GND	LCD logic and driver ground
16	LCD_GND	LCD logic and driver ground
17	HPD	HPD signale pin
18	BL_GND	Backlight ground
19	BL_GND	Backlight ground
20	BL_GND	Backlight ground
21	BL_GND	Backlight ground
22	BL_Enable	Backlight On / Off
23	BL_PWM_DIM	System PWM signal Input
24	NC	Reverse for AUO TEST only
25	NC	Reverse for AUO TEST only
26	BL_PWR	Backlight power (6V~21V)
27	BL_PWR	Backlight power (6V~21V)
28	BL_PWR	Backlight power (6V~21V)
29	BL_PWR	Backlight power (6V~21V)
30	NC	No Connect



Note1: Start from right side.

Note2: Input signals shall be low or High-impedance state when VDD is off.
Internal circuit of **eDP inputs** are as following.



6.3 Interface Timing

6.3.1 Timing Characteristics

Basically, interface timings should match the 1600x900 /60Hz manufacturing guide line timing.

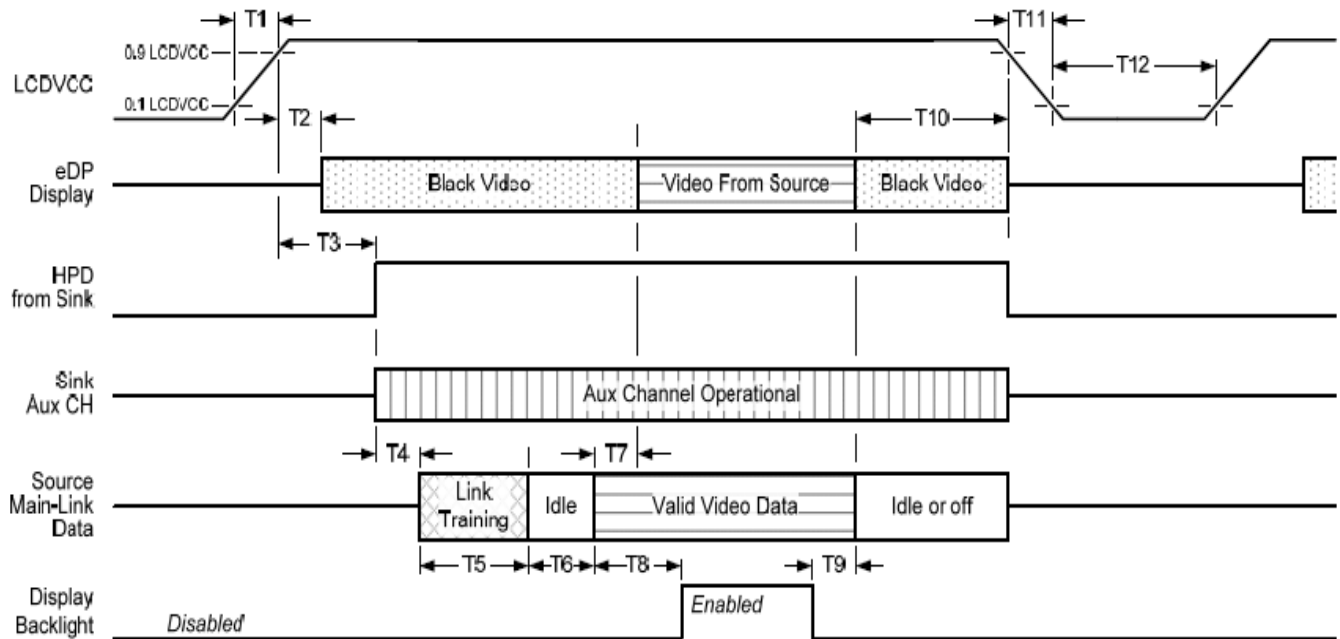
Parameter	Symbol	Min.	Typ.	Max.	Unit	
Frame Rate	-		60		Hz	
Clock frequency	$1/ T_{\text{Clock}}$		56.3		MHz	
Vertical Section	Period	T_V	908	930	900+A	T_{Line}
	Active	T_{VD}	900			
	Blanking	T_{VB}	8	30	A	
Horizontal Section	Period	T_H	830	1016	800+B	T_{Clock}
	Active	T_{HD}	800			
	Blanking	T_{HB}	30	216	B	

Note 1 : The above is as optimized setting

Note 2 : The maximum clock frequency = $(800+B)*(900+A)*60 < 80\text{MHz}$

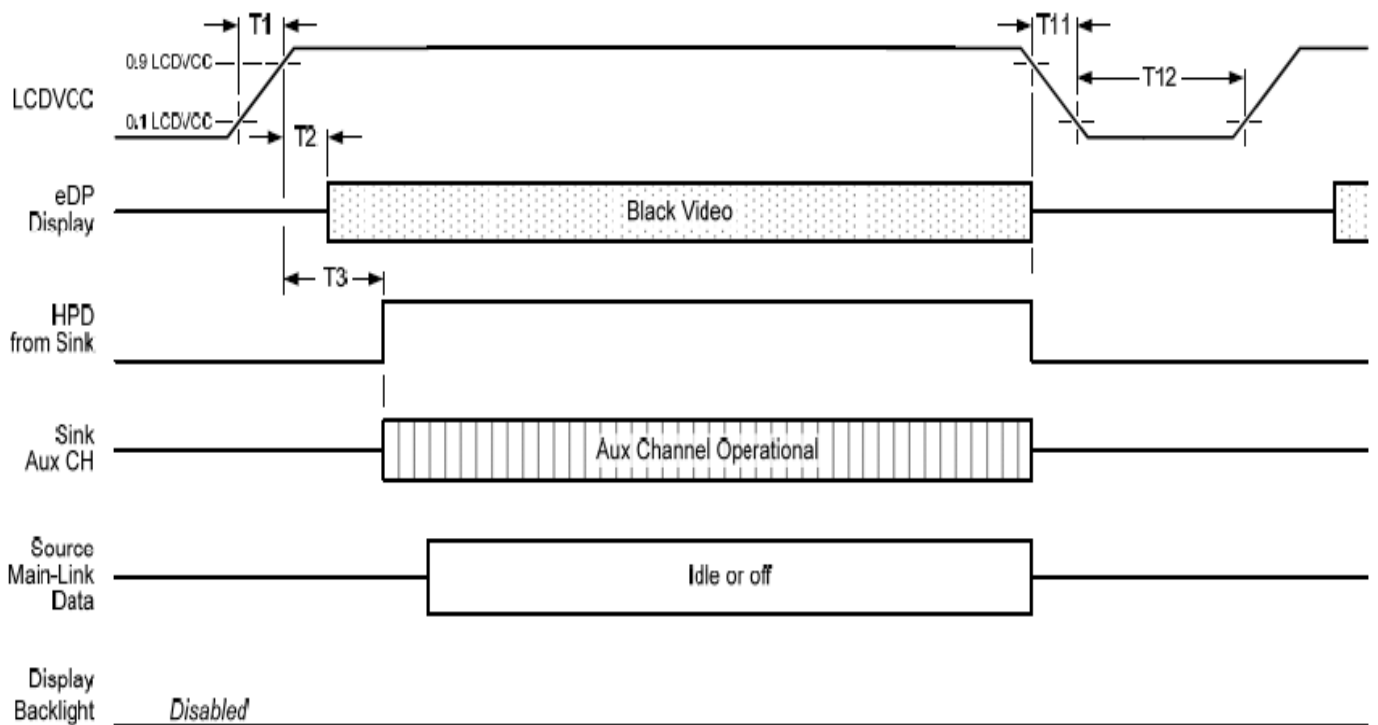
6.4 Power ON/OFF Sequence

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only



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Display Port panel power sequence timing parameter:

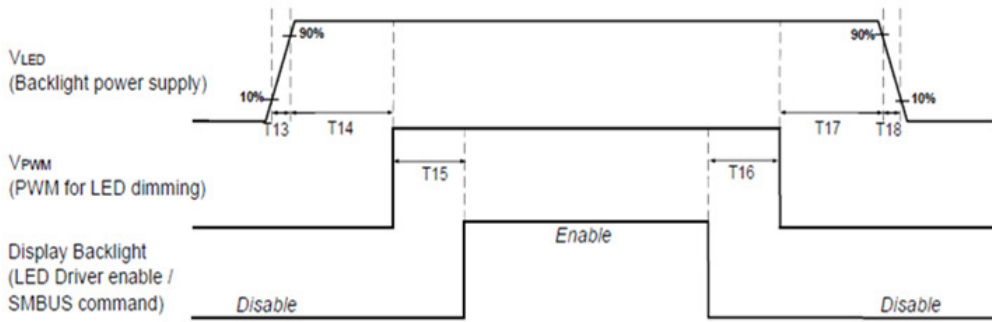
Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 90% to 10%	source			10ms	
T12	power off time	source	500ms			

Note 1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
 -upon LCDVDD power on (within T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
 -when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

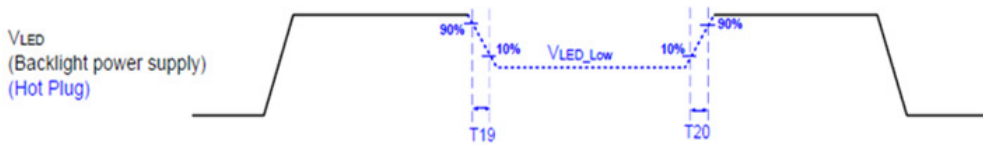
Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Display Port panel B/L power sequence timing parameter:



Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	10	-
T16	10	-
T17	10	-
T18	0.5	10
T19	1*	-
T20	1*	-

Seamless change: $T19/T20 = 5 \times T_{PWM}^*$

* $T_{PWM} = 1/PWM \text{ Frequency}$

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40°C, 90%RH, 300h	
High Temperature Operation	Ta= 50°C, Dry, 300h	
Low Temperature Operation	Ta= 0°C, 300h	
High Temperature Storage	Ta= 60°C, 35%RH, 300h	
Low Temperature Storage	Ta= -20°C, 50%RH, 250h	
Thermal Shock Test	Ta=-20°C to 60°C, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. Self-recoverable.
No data lost, No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

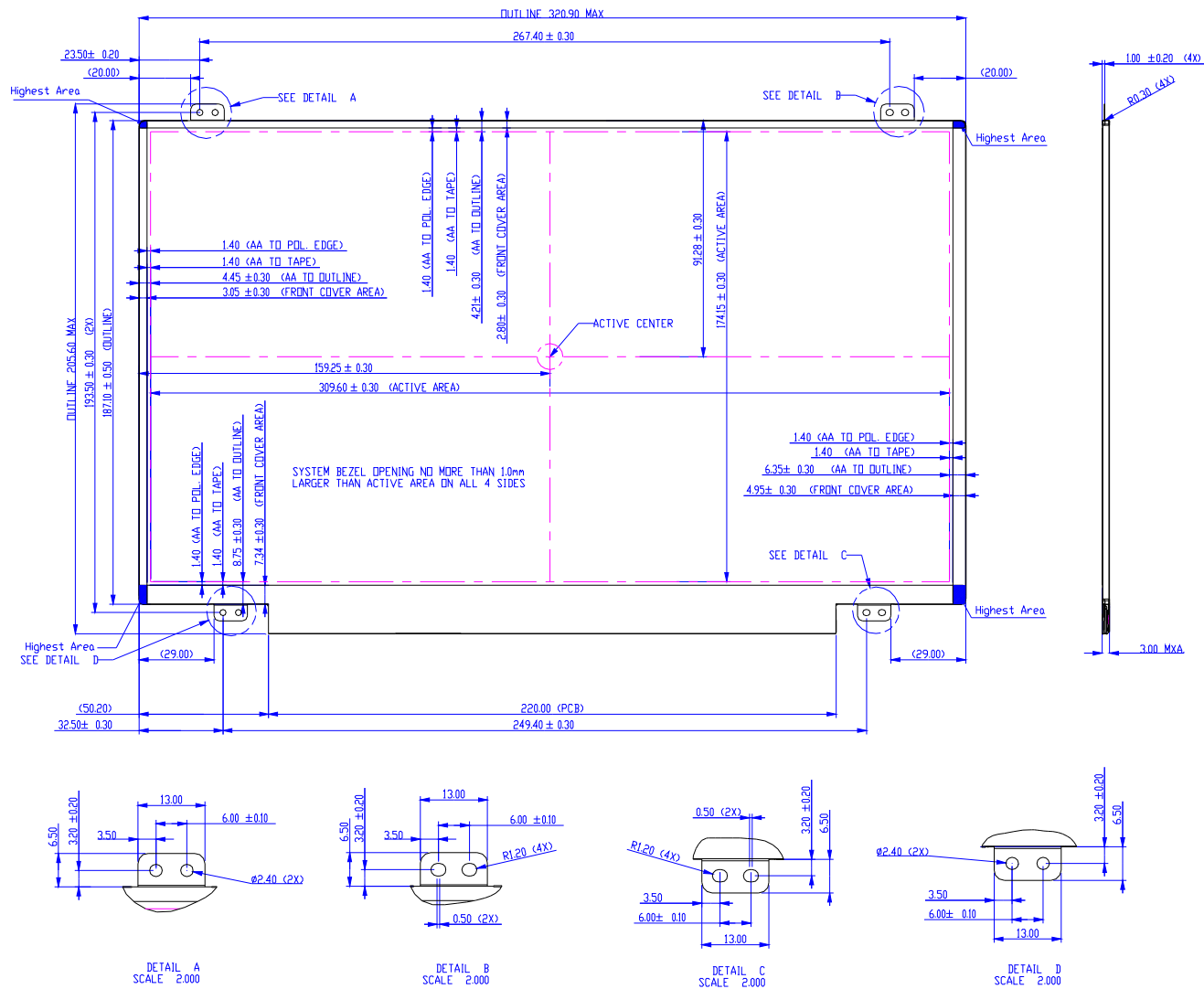


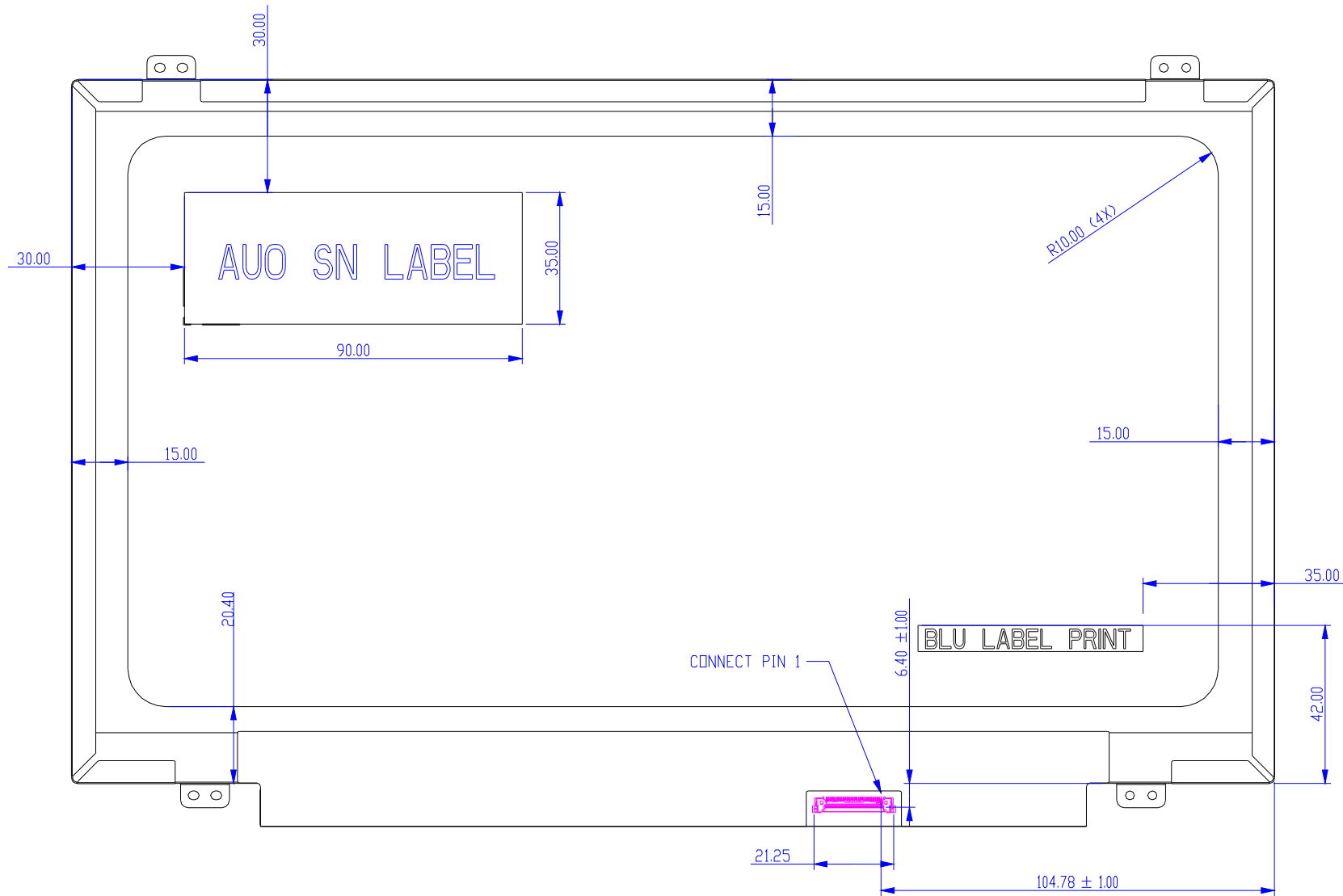
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8. Mechanical Characteristics

8.1 LCM Outline Dimension





Note: Prevention IC damage, IC positions not allowed any overlap over these areas.

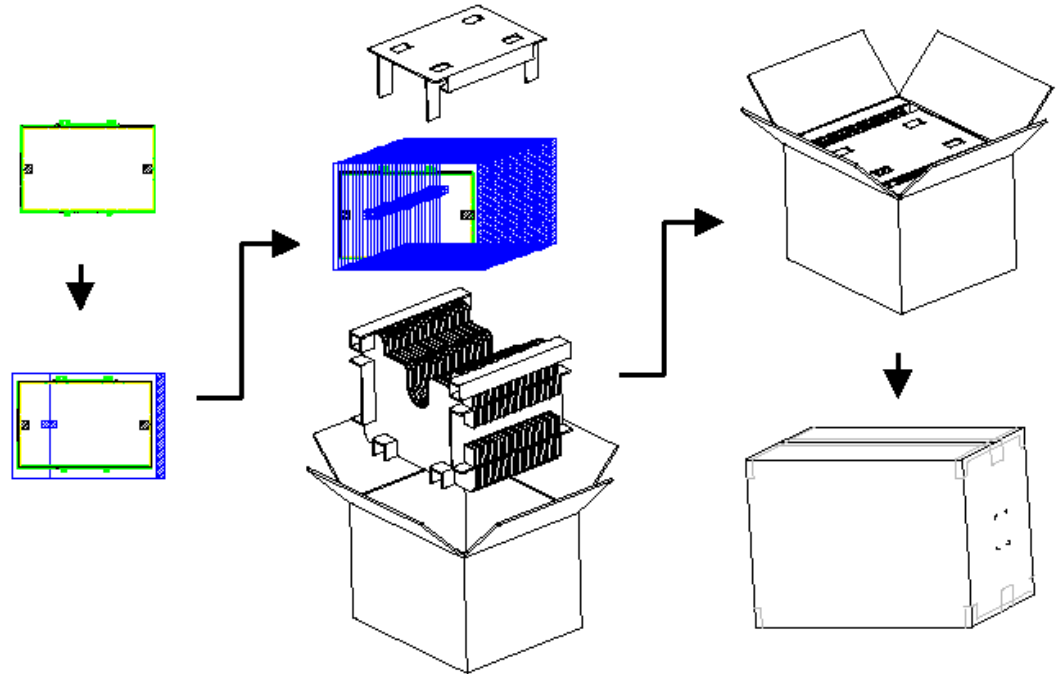


9. Shipping and Package

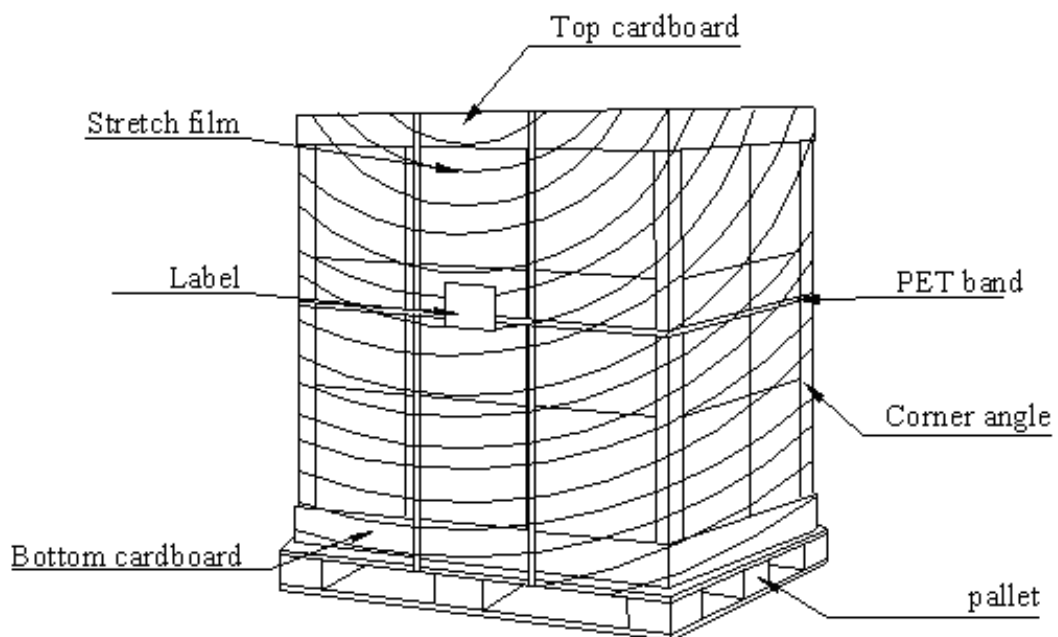
9.1 Shipping Label Format

TBD

9.2 Carton Package



9.3 Shipping Package of Palletizing Sequence





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10. Appendix: EDID Description

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	3E	00111110	62	
0B	hex, LSB first	30	00110000	48	
0C	32-bit ser #	00	00000000	0	
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of manufacture	00	00000000	0	
11	Year of manufacture	16	00010110	22	
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	04	00000100	4	
14	Video input def. (<i>digital I/P, non-TMDS, CRGB</i>)	95	10010101	149	
15	Max H image size (<i>rounded to cm</i>)	1F	00011111	31	
16	Max V image size (<i>rounded to cm</i>)	11	00010001	17	
17	Display Gamma (<i>=(gamma*100)-100</i>)	78	01111000	120	
18	Feature support (<i>no DPMS, Active OFF, RGB, tmg Blk#1</i>)	02	00000010	2	
19	Red/green low bits (Lower 2:2:2:2 bits)	A0	10100000	160	
1A	Blue/white low bits (Lower 2:2:2:2 bits)	95	10010101	149	
1B	Red x (Upper 8 bits)	99	10011001	153	
1C	Red y/ highER 8 bits	59	01011001	89	
1D	Green x	52	01010010	82	
1E	Green y	92	10010010	146	
1F	Blue x	26	00100110	38	
20	Blue y	21	00100001	33	
21	White x	50	01010000	80	
22	White y	54	01010100	84	
23	Established timing 1	00	00000000	0	
24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	
26	Standard timing #1	01	00000001	1	
27		01	00000001	1	
28	Standard timing #2	01	00000001	1	
29		01	00000001	1	
2A	Standard timing #3	01	00000001	1	



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2B		01	00000001	1	
2C	Standard timing #4	01	00000001	1	
2D		01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F		01	00000001	1	
30	Standard timing #6	01	00000001	1	
31		01	00000001	1	
32	Standard timing #7	01	00000001	1	
33		01	00000001	1	
34	Standard timing #8	01	00000001	1	
35		01	00000001	1	
36	Pixel Clock/10000 LSB	FC	11111100	252	
37	Pixel Clock/10000 USB	2B	00101011	43	
38	Horz active Lower 8bits	40	01000000	64	
39	Horz blanking Lower 8bits	A0	10100000	160	
3A	HorzAct:HorzBlnk Upper 4:4 bits	61	01100001	97	
3B	Vertical Active Lower 8bits	84	10000100	132	
3C	Vertical Blanking Lower 8bits	1E	00011110	30	
3D	Vert Act : Vertical Blanking (upper 4:4 bit)	30	00110000	48	
3E	HorzSync. Offset	40	01000000	64	
3F	HorzSync.Width	2A	00101010	42	
40	VertSync.Offset : VertSync.Width	33	00110011	51	
41	Horz&Vert Sync Offset/Width Upper 2bits	00	00000000	0	
42	Horizontal Image Size Lower 8bits	35	00110101	53	
43	Vertical Image Size Lower 8bits	AE	10101110	174	
44	Horizontal & Vertical Image Size (upper 4:4 bits)	10	00010000	16	
45	Horizontal Border <i>(zero for internal LCD)</i>	00	00000000	0	
46	Vertical Border <i>(zero for internal LCD)</i>	00	00000000	0	
47	Signal <i>(non-intr, norm, no stero, sep sync, neg pol)</i>	18	00011000	24	
48	Pixel Clock/10,000 (LSB)	53	01010011	83	40Hz frame rate
49	Pixel Clock/10,000 (MSB)	1D	00011101	29	
4A	Horizontal Addressable Pixels, lower 8 bits	40	01000000	64	
4B	Horizontal Blanking Pixels, lower 8 bits	A0	10100000	160	
4C	H Pixels, upper nibble : H Blanking, upper nibble	61	01100001	97	
4D	Vertical Addressable Lines, lower 8 bits	84	10000100	132	
4E	Vertical Blanking Lines, lower 8 bits	1E	00011110	30	
4F	V lines, upper nibble : V blanking, upper nibble	30	00110000	48	
50	Horizontal Front Porch, lower 8 bits	40	01000000	64	
51	Horizontal Sync Pulse, lower 8 bits	2A	00101010	42	
52	V Front Porch, lower nibble : V Sync Pulse, lower nibble	33	00110011	51	
53	VFP, 2 bits: VSP 2 bits: HFP 2 bits: HFP 2 bits	00	00000000	0	
54	Horizontal Image Size in mm, lower 8 bits	35	00110101	53	
55	Vertical Image Size in mm, lower 8 bits	AE	10101110	174	
56	H Image Size, upper nibble : V Image Size, upper nibble	10	00010000	16	
57	Horizontal Border	00	00000000	0	
58	Vertical Border	00	00000000	0	
59	Bit Encode Sync Information	18	00011000	24	



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5A	DC	00	00000000	0	nVDPS Reserved 00	
5B	HTOTAL	00	00000000	0		
5C	HA	00	00000000	0		
5D	HBL	00	00000000	0		
5E	HFP	00	00000000	0		
5F	HFPe	00	00000000	0		
60	HBP	00	00000000	0		
61	HB	00	00000000	0		
62	HSO	00	00000000	0		
63	HS	00	00000000	0		
64	VTOTAL	00	00000000	0		
65	VA	00	00000000	0		
66	VBL	00	00000000	0		
67	VFP	00	00000000	0		
68	VBP	00	00000000	0		
69	VB	00	00000000	0		
6A	VSO	00	00000000	0		
6B	VS	00	00000000	0		
6C	Detail Timing Description #4	00	00000000	0		Header
6D	Flag	00	00000000	0		
6E	Reserved	00	00000000	0		
6F	For Brightness Table and Power Consumption	02	00000010	2		
70	Flag	00	00000000	0		Brightness Table
71	PWM % [7:0] @ Step 0	0C	00001100	12		
72	PWM % [7:0] @ Step 5	3D	00111101	61		
73	PWM % [7:0] @ Step 10	FF	11111111	255		
74	Nits [7:0] @ Step 0	0A	00001010	10		
75	Nits [7:0] @ Step 5	3C	00111100	60		
76	Nits [7:0] @ Step 10	7D	01111101	125	Power Consumption	
77	Panel Electronics Power @ 32x32 Chess Pattern =	1B	00011011	27		
78	Backlight Power @ 60 nits =	11	00010001	17		
79	Backlight Power @ Step 10 =	24	00100100	36		
7A	Nits @ 100% PWM Duty =	7D	01111101	125		
7B	Flag	20	00100000	32		
7C	Flag	20	00100000	32		
7D	Flag	20	00100000	32		
7E	Extension Flag	00	00000000	0		
7F	Checksum	3C	00111100	60		